Q.P. Code: 19CS0504 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Regular Examinations Feb-2021

COMPUTER ORGANIZATION & ARCHITECTURE

(Common to CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	List out the Computer Instructions and Explain about it.	**8M**
	b	Differentiate between I/O unit and memory Unit.	**4M**

OR

2		Illustrate any four addressing modes with neat sketch.	**12M**

UNIT-II

3		Illustrate the steps in Booth multiplication algorithm and Draw the flowchart with an example	**12M**

OR

4	**a**	Compare signed number, 1's complement, 2's complement with an example.	**4M**
	b	Describe about fixed and floating point representations	**8M**

UNIT-III

5	**a**	Examine the Bus transfer with neat diagram.	**6M**
	b	Summarize the Register Representations and way it is used.	**6M**

OR

6		Describe the Micro Programmed Control with a neat sketch.	**12M**

UNIT-IV

7	**a**	Define track and sector. Analyze the importance of auxiliary memory.	**6M**
	b	Compare various types of Auxiliary memory	**6M**

OR

8	**a**	Assess the Memory Hierarchy with neat sketch.	**8M**
	b	Discuss briefly about synchronous DRAMs.	**4M**

UNIT-V

9		Describe the Interconnection Structures in detail.	**12M**

OR

10	**a**	Anticipate the conflicts in pipelining and describe about it.	**6M**
	b	Construct 4-segment Instruction Pipeline and explain.	**6M**

*** END ***